CLAIMS

What is claimed is:

1. A computer system, comprising:

a computer bus coupling together a plurality of bus devices;

a bus arbiter coupled to the computer bus, said bus arbiter receiving requests from said plurality of bus devices to obtain access to the computer bus;

wherein said bus arbiter resolves conflicting requests from said bus devices based on the workload of the bus devices that request access to the computer bus.

2. The system of claim 1, wherein each of said plurality of bus devices includes a queue in which pending operations are stored while the bus device awaits access to the computer bus.

3. The system of claim 2, wherein each of said plurality of bus devices asserts a signal to said bus arbiter when one or more operations are pending in the queue.

4. The system of claim 3, wherein each of said plurality of bus devices also asserts a signal to said bus arbiter indicating the number of operations pending in the queue.

5. The system of claim 4, wherein said bus arbiter compares the signal indicating the number of operations pending in the queue from any bus devices requesting access to the computer bus, and awards access to the computer bus to the bus device with the most operations pending in its associated queue.

6. The system of claim 5, wherein said bus arbiter breaks any ties between bus devices with an equal number of operations pending in the queue based on a predetermined priority value assigned to each bus device.

7. The system of claim 5, wherein said bus arbiter breaks any ties between bus devices with an equal number of operations pending in the queue based on the length of time since each device was last granted access to the computer bus.

8. The system of claim 5, wherein the signal indicating the number of operations pending in the queue comprises a multi-bit signal.

9. The system of claim 8, wherein the multi-bit signal comprises n bits, with 2^n = number of entries in the queue of each device.

10. The system of claim 3, wherein each of said plurality of bus devices also asserts a signal to said bus arbiter indicating a range of operations pending in the queue.

11. A computer system, comprising:

a bus ;

a plurality of bus devices, each of which couples to said bus, and each of which is capable of running cycles on said bus and each of said bus devices includes a queue in which pending operations are stored while the bus device awaits access to the bus;

a bus arbiter coupled to the bus, said bus arbiter receiving request signals from said plurality of bus devices that are seeking to run a cycle on said bus;

wherein any of said devices that include one or more operations in its queue transmits a signal to said bus arbiter requesting access to said bus and indicating the number of operations pending in its associated queue; and

wherein said bus arbiter resolves conflicting requests from said bus devices based on the number of operations pending in the queues of the requesting devices.

12. The system of claim 11, wherein each of said plurality of bus devices is capable of running bus cycles on said bus, and wherein said signal requesting access to said bus is a request for ownership of said bus.

13. The system of claim 11, wherein any bus devices with operations pending in a queue transmit a request signal indicating a request for access to said bus, and a workload signal indicating the number of operations pending in the queue.

14. The system of claim 13, wherein each bus device has a queue with the same number of entries.

15. The system of claim 13, wherein at least two of said bus devices have queues with a different number of entries.

16. A method of resolving conflicting bus access requests in a computer bus, comprising the acts of:

determining if more than one bus device has requested access to the computer bus;

determining the workload associated with each bus device requesting access to the computer bus; and

granting access to the bus device that has the greatest workload.

17. The method of claim 16, wherein the act of determining if more than one bus device has requested access includes monitoring for a request signal from each of the bus devices capable of initiating cycles on the computer bus.

18. The method of claim 16, wherein the act of determining the workload associated with each bus device includes receiving a signal from each device indicating the number of operations awaiting execution in that device.

19. The method of claim 18, wherein the number of operations awaiting execution is determined based on the number of operations pending in a queue in that device.

20. The system of claim 16, further comprising the act of breaking any ties between devices with equal workloads based on other priority criteria.